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Addition/Correction

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Correction to ZnO/NiO Diode-Based Charge Trapping Layer for Flash Memory Featuring Low Voltage Operation

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ACS Appl. Mater. Interfaces **2015**, *7*, pp 6383−6390. DOI: 10.1021/am507535c

Recently, we found that in Figure 3c, d, the band diagram for program and erase operation, respectively, were

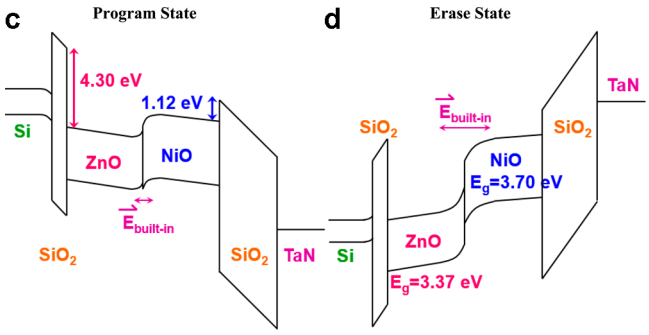

Figure 3. Band diagram for memory devices with ZnO/NiO charge trapping layer biased at (c) positive gate voltage and (d) negative gate voltage.

mistakenly uploaded. The band diagram of the charge-trapping layer ZnO/NiO should be switched so that the diagrams can be consistent with the operation mechanism described in the paper. The corrected band diagrams are shown below. The conclusions of the paper are not influenced by this change.

Published: April 29, 2015

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DOI: 10.1021/acsami.5b03117
ACS Appl. Mater. Interfaces 2015, 7, 10067−10067